AMENDMENTS TO THE CLAIMS

1) (Currently amended) A ~~micro-machined~~ structure comprising:

a structural layer ~~consisting essentially of sputtered silicon, said structural layer comprising~~ having

a core sputtered silicon layer patterned with released structures thereof;

a first conductive layer in contact with and on top of said core sputtered silicon layer; and

a second conductive layer in contact with and below said core sputtered silicon layer, wherein said first and second conductive layers have essentially the same shape as said core sputtered silicon layer; and

a ~~pre-fabricated integrated electronic~~ complimentary metal oxide semiconductor circuitry ~~electrically coupled to~~ integrated with said structural layer, wherein said ~~pre-fabricated integrated electronic circuitry is characterized as an operational~~ semiconductor circuitry has a metalized circuitry layer on top of an oxidized layer of a substrate.

2) (Cancelled).

3) (Currently amended) The ~~micro-machined~~ structure of claim ~~2~~ 1, wherein

~~said~~ at least one of said first and second conductive layers is made from a Titanium based material.

4) (Currently amended) The ~~micro-machined~~ structure of claim ~~2~~ 3, wherein

said ~~at least one conductive layer is made from a~~ Titanium based material is selected from a group consisting of TiW and TiN.

5) (Cancelled).

6) (Currently amended) The ~~micro-machined~~ structure of claim ~~2~~ 1, wherein

said core sputtered silicon layer has a first dissolving characteristic and ~~said~~ at least one or both of said first and second conductive layers has a second dissolving characteristic and wherein said second dissolving characteristic is compatible with said first dissolving characteristic.

7) (Currently amended) The ~~micro-machined~~ structure of claim 1, wherein said ~~operational~~ semiconductor circuitry includes an aluminum-based metalization.

8) (Cancelled).

9) (Currently amended) ~~The micro-machined~~ A structure ~~of claim 1, further~~ comprising:
a substrate;
a sacrificial layer on top of said substrate;
a core sputtered silicon layer on top of said sacrificial layer, wherein said core sputtered silicon layer is patterned with released structures thereof;
a released area defined by said substrate, said sacrificial layer, and said core sputtered silicon layer;
metalized circuitry elements on top of said core sputtered silicon layer; and
at least one sealing layer covering said released area.

10) (Currently amended) The ~~micro-machined~~ structure of claim 9, wherein said at least one sealing layer ~~consisting essentially of~~ is silicon nitride.

11) (Currently amended) The ~~micro-machined~~ structure of claim 1 or 9, wherein said core sputtered silicon layer is made from boron doped silicon.

12) (Currently amended) The ~~micro-machined~~ structure of claim 1 or 9, wherein said core sputtered silicon layer is made from silicon doped with 40-80 ppm boron.

13) (Currently amended) The ~~micro-machined~~ structure of claim 1 or 9, wherein said ~~micro-machined structure is characterized as having an~~ released structures are essentially buckling-free ~~deformation configuration~~.

14) (Currently amended) The ~~micro-machined~~ structure of claim 1 or 9, wherein said core sputtered silicon layer has a predetermined thickness which influences a strain gradient of said ~~micro-machined~~ structure.

15) (Cancelled).

16) (Currently amended) The ~~micro-machined~~ structure of claim 1, wherein said ~~micro-machined~~ structure ~~is characterized as having~~ has a variable sputtered layer thickness and a correlated curvature, wherein said correlated curvature essentially decreases with an increase of the variable sputtered layer thickness.

Claims 17-41 (Cancelled).